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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	(714/741.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:36
L2	7	(714/726.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:36
L3	0	(714/717.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L4	6	(714/738.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L5	9	(714/724.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:37
L6	0	(714/48.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:38
L7	45	(716/16.ccls.) and emulation and ((configur$5 or program$4) with ((logic adj block$1) or FPGA)) and test$3	US-PGPUB; USPAT; USOCR	OR	OFF	2008/01/23 10:38
S146	2	(inverse adj routing) with configuration	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/19 16:37
S151	1	inverse with routing with ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:01
S152	1	inverse with routing same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:01

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S153	19	(inverse with rout$3) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:17
S154	1	(inverse adj rout$3) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 12:03
S156	55	loopback with output with result	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 14:57
S158	5	(loopback with output with result) and (fail$3 with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:02
S159	1	((loopback with output with result) same logic) and (fail$3 with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:03
S160	48	((loopback with output) same logic) and (fail$3 with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:07
S161	2	((loopback with output) same logic same (fail$3 with indicat$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:11
S162	1	((loopback with output) same logic same FPGA) and (fail$3 with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:13

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S163	1	((loopback with output) same FPGA) and (fail$3 with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:14
S164	16	(loopback with output) and (fail$3 with indicat$3) and FPGA and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:20
S167	16	(loopback with output) and (fail$3 with indicat$3) and FPGA and logic	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:27
S169	38	(loopback with output) and (fail$3 with indicat$3) and (logic with configur$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:30
S170	3	(loopback with output with result) and (fail$3 with indicat$3) and (logic with configur$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:50
S171	3	(loopback with output with result) and (logic with configur$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 15:56
S172	1	(loopback with output with indicator)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 16:00
S174	37	(loopback with failure with indicat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:02

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S176	4	(loopback with failure with indicat$3) and FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 16:02
S178	1	(inverse with routing) same ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:20
S179	52	(inverse with routing) and ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:33
S180	4	(inverse adj routing) and ((integrated adj circuit) or IC)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/01/20 18:33

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- Combine search queries using AND, OR, or NOT
- Delete a search
- Run a search

Wed, 23 Jan 2008, 10:50:40 AM EST

Search Query Display

Recent Search Queries

		Results
#1	(configurable logic block<and>verifier)<and>failure indicator	0
#2	(testing routing<and>input data)<and>inverse configuration	0

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